
Features

- Operates as Host or Device Bridge Between Serial ATA and Parallel ATA interfaces
- Ultra ATA100 Mode Supported with Rates up to 100 MB/s
- Data is Transferred on Both Edges of the STROBE when in Ultra DMA Mode
- 16-bit CRC is Calculated on a Per-burst Basis
- Ultra DMA5 Compliant Drive Interfaces
- Compatible with 48-bit LBA Methods of Addressing
- Dual 1024-byte Transmit/Receive FIFO for Overrun Prevention
- 8B/10B Encoding and Decoding in Serial ATA Link Layer
- Low Power: < 380 mW
- Supports PIO Modes 0, 1, 2, 3 and 4
- Supports UDMA Modes 0, 1, 2, 3, 4, and 5
- Supports 80-conductor Cable for UDMA Modes 4, and 5

Overview

The AT78C5010 SATA Controller bridges the conventional Parallel ATA devices with Serial ATA PHY transceivers. It includes a Serial ATA Link layer, a Transport layer, a Command Layer, two 256 x 32 FIFOs and an IDE Host/Target Controller, a Serial ATA Core and an IDE Controller, and is fully compliant with Serial ATA Gen1. The PHY block is connected to the ATA block by a 20-bit transmit and a 20-bit receive data bus. The bridge is intended to adapt an Ultra ATA100 Disk drive to a Serial ATA Host interface, and a Serial ATA Device interface to Ultra ATA100 Host interface. Ultra DMA is a data transfer protocol used with the READ DMA, WRITE DMA, READ DMA QUEUED, WRITE DMA QUEUED, and PACKET commands.



Serial ATA Host/Device Bridge

AT78C5010

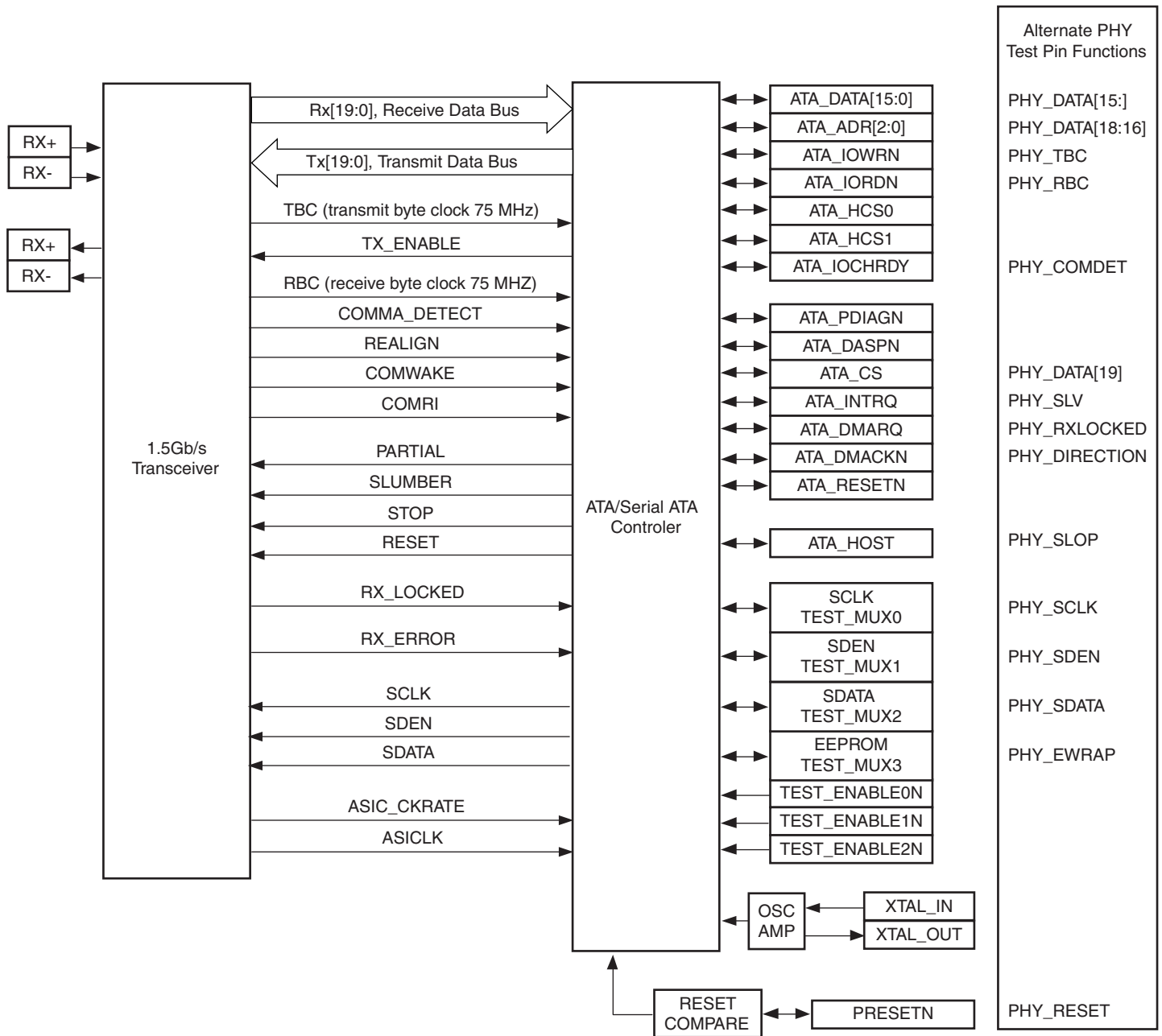
Summary

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Note: This is a summary document. A complete document is available under NDA. For more information, please contact your local Atmel sales office.

Figure 1. AT78C5010 Block/PAD Interconnect





Atmel Corporation

2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 487-2600

Regional Headquarters

Europe

Atmel Sarl
Route des Arsenalux 41
Case Postale 80
CH-1705 Fribourg
Switzerland
Tel: (41) 26-426-5555
Fax: (41) 26-426-5500

Asia

Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimshatsui
East Kowloon
Hong Kong
Tel: (852) 2721-9778
Fax: (852) 2722-1369

Japan

9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
Tel: (81) 3-3523-3551
Fax: (81) 3-3523-7581

Atmel Operations

Memory

2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

Microcontrollers

2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

La Chantrerie
BP 70602
44306 Nantes Cedex 3, France
Tel: (33) 2-40-18-18-18
Fax: (33) 2-40-18-19-60

ASIC/ASSP/Smart Cards

Zone Industrielle
13106 Rousset Cedex, France
Tel: (33) 4-42-53-60-00
Fax: (33) 4-42-53-60-01

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906, USA
Tel: 1(719) 576-3300
Fax: 1(719) 540-1759

Scottish Enterprise Technology Park
Maxwell Building
East Kilbride G75 0QR, Scotland
Tel: (44) 1355-803-000
Fax: (44) 1355-242-743

RF/Automotive

Theresienstrasse 2
Postfach 3535
74025 Heilbronn, Germany
Tel: (49) 71-31-67-0
Fax: (49) 71-31-67-2340

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906, USA
Tel: 1(719) 576-3300
Fax: 1(719) 540-1759

Biometrics/Imaging/Hi-Rel MPU/ High Speed Converters/RF Datacom

Avenue de Rochepleine
BP 123
38521 Saint-Egreve Cedex, France
Tel: (33) 4-76-58-30-00
Fax: (33) 4-76-58-34-80

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www.atmel.com/literature

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